**Status of the claims:**

1. (Previously presented) An integrated circuit comprising:

a standard dimension carrier substrate;

an information router integrated on the carrier substrate; and

system memory operative to store system instructions also integrated on the carrier substrate and in electrical communication with the information router via at least one of a plurality of electrical leads associated with the carrier substrate, wherein the system instructions may be stored and retrieved from the system memory through the information router.

2. (Original) The integrated circuit of claim 1 wherein the information router is disposed within an application specific integrated circuit die.

3. (Original) The integrated circuit of claim 2 further comprising:

a graphics controller further disposed within the application specific integrated circuit die in conjunction with the information router.

4. (Original) The integrated circuit of claim 3 further comprising:

graphics memory also integrated on the carrier substrate and in electrical communication with the graphics controller via at least one of the plurality of electrical leads associated with the carrier substrate, wherein graphics information may be stored and retrieved from the graphics memory.

5. (Original) The integrated circuit of claim 2 wherein the application specific integrated circuit die is coupled to at least one of the plurality of electrical leads associated with the carrier substrate using a plurality of wirebonds.

6. (Original) The integrated circuit of claim 2 wherein the system memory is disposed on a top surface of the carrier substrate and the application specific integrated circuit die is coupled to a bottom surface of the carrier substrate of the packaged chip using a flip chip technology.

7. (Original) The integrated circuit of claim 1 wherein the system memory is disposed within a chip scale package memory having a plurality of contact pins, wherein the contact pins are soldered to the carrier substrate.

8. (Original) The integrated circuit of claim 1 wherein the system memory is a memory die coupled to the carrier substrate using a plurality of wirebonds.

9. (Original) The integrated circuit of claim 1 wherein the information router within the application specific integrated circuit die is capable of being operably coupled to a central processing unit across a printed circuit board.

10. (Previously presented) An integrated circuit comprising:

a standard dimension carrier substrate having a plurality of electrical leads disposed between a top surface and a bottom surface of the carrier substrate;

an application specific integrated circuit die coupled to the bottom surface of the carrier substrate, wherein the application specific integrated circuit die includes a north bridge; and

system memory operative to store system instructions, the system memory integrated on the top surface of the carrier substrate and in electrical communication with the north bridge via at least one of the plurality of electrical leads within the carrier substrate, wherein the system instructions may be stored and retrieved from the system memory through the north bridge, within the packaged chip.

11. (Original) The integrated circuit of claim 10 wherein the application specific integrated circuit die further includes a graphics controller in conjunction with the north bridge.

12. (Original) The integrated circuit of claim 11 further comprising:

graphics memory also integrated on the carrier substrate and in electrical communication with the graphics processor via at least one of the plurality of electrical leads within the carrier substrate, wherein graphics information may be stored and retrieved from the graphics memory, within the packaged chip.

13. (Original) The integrated circuit of claim 10 wherein the application specific integrated circuit die is coupled to the bottom surface of the carrier substrate using a plurality of wirebonds.

14. (Original) The integrated circuit of claim 10 wherein the system memory is disposed within at least one chip scale package memory having a plurality of contact pins, wherein the contact pins are soldered to the carrier substrate.

15. (Original) The integrated circuit of claim 10 wherein the system memory is at least one memory die coupled to the carrier substrate using a plurality of wirebonds.

16. (Original) The integrated circuit of claim 10 wherein the north bridge within the application specific integrated circuit die is capable of being operably coupled to a central processing unit across a printed circuit board.

17—20.(Cancelled)